The SN54HCT244 and SN74HCT244 are octal buffers and line drivers with 3-state outputs. They are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices are organized as two 4-bit buffers/drivers with separate output-enable (OE) inputs. When OE is low, the device passes noninverted data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

### Ordering Information

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40°C to 85°C</td>
<td>PDIP – N</td>
<td>Tube of 20</td>
<td>SN74HCT244N</td>
</tr>
<tr>
<td></td>
<td>SOIC – DW</td>
<td>Tube of 25</td>
<td>SN74HCT244DW</td>
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<tr>
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<td>SOP – NS</td>
<td>Reel of 2000</td>
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<td>SSOP – DB</td>
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<td>Reel of 2000</td>
<td>SN74HCT244PWR</td>
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</tr>
<tr>
<td></td>
<td>CFP – W</td>
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<td></td>
<td>LCCC – FK</td>
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</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
FUNCTION TABLE
(each buffer/driver)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
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<tr>
<td>OE</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
</tbody>
</table>

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Supply voltage range, $V_{CC}$: $-0.5 \text{ V}$ to $7 \text{ V}$
- Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1): $\pm 20 \text{ mA}$
- Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1): $\pm 20 \text{ mA}$
- Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$): $\pm 35 \text{ mA}$
- Continuous current through $V_{CC}$ or GND: $\pm 70 \text{ mA}$
- Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package: $70 \text{ °C/W}$
  DW package: $58 \text{ °C/W}$
  N package: $69 \text{ °C/W}$
  NS package: $60 \text{ °C/W}$
  PW package: $83 \text{ °C/W}$
- Storage temperature range, $T_{stg}$: $-65 \text{ °C}$ to $150 \text{ °C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
recommended operating conditions (see Note 3)

| PARAMETER | TEST CONDITIONS | \( V_{CC} \) | \( T_A = 25^\circ C \) | \( V_{IH} \) | \( V_{IL} \) | \( V_{OL} \) | \( I_I \) | \( I_O \) | \( I_{CC} \) | \( \Delta I_{CC} \)† | \( C_i \) |
|-----------|----------------|--------------|----------------|----------|----------|----------|-----------|---------|---------|--------|--------|-------|
| \( V_{OH} \) | \( V_I = V_{IH} \) or \( V_{IL} \) | \( -20 \mu A \) | 4.5 V | 4.4 | 4.499 | 4.4 | 4.4 | 4.4 | 4.4 | V | 4.5 V to 5.5 V |
| \( V_{OL} \) | \( V_I = V_{IH} \) or \( V_{IL} \) | \( 20 \mu A \) | 4.5 V | 0.001 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V | 4.5 V to 5.5 V |
| \( I_I \) | \( V_I = V_{CC} \) or 0 | \( -6 mA \) | 5.5 V | ±0.1 | ±100 | ±1000 | ±1000 | ±1000 | ±5 | μA | 5.5 V |
| \( I_O \) | \( V_O = V_{CC} \) or 0, \( V_I = V_{IH} \) or \( V_{IL} \) | \( 6 mA \) | 5.5 V | ±0.01 | ±0.5 | ±10 | ±10 | ±5 | μA | 5.5 V |
| \( I_{CC} \) | \( V_I = V_{CC} \) or 0, \( I_O = 0 \) | 5.5 V | 8 | 160 | 80 | 2.9 | mA | 5.5 V |
| \( \Delta I_{CC} \)† | One input at 0.5 V or 2.4 V, Other inputs at 0 or \( V_{CC} \) | 5.5 V | 1.4 | 2.4 | 3 | 2.9 | mA | 5.5 V |
| \( C_i \) | 4.5 V to 5.5 V | 3 | 10 | 10 | 10 | 10 | pF | 4.5 V to 5.5 V |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or \( V_{CC} \).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>( T_A = 25^\circ C )</th>
<th>( V_{OH} )</th>
<th>( V_{OL} )</th>
<th>( I_I )</th>
<th>( I_O )</th>
<th>( I_{CC} )</th>
<th>( \Delta I_{CC} )†</th>
<th>( C_i )</th>
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</thead>
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<td>( t_{pd} )</td>
<td>( A )</td>
<td>( Y )</td>
<td>4.5 V</td>
<td>15</td>
<td>28</td>
<td>42</td>
<td>35</td>
<td>ns</td>
<td>4.5 V to 5.5 V</td>
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<td>( OE )</td>
<td>( Y )</td>
<td>4.5 V</td>
<td>13</td>
<td>25</td>
<td>38</td>
<td>32</td>
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<td>4.5 V to 5.5 V</td>
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<tr>
<td>( t_{dis} )</td>
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<td>( Y )</td>
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<tr>
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<td>( Y )</td>
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<td>12</td>
<td>18</td>
<td>15</td>
<td>ns</td>
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switching characteristics over recommended operating free-air temperature range, \( C_L = 50 \) pF (unless otherwise noted) (see Figure 1)
SN54HCT244, SN74HCT244
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
SCLS175D – MARCH 1984 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range, \( C_L = 150 \text{ pF} \) (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CC} )</th>
<th>( T_{A} = 25^\circ\text{C} )</th>
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<th>SN74HCT244</th>
<th>UNIT</th>
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<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
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<td>Y</td>
<td>4.5 V</td>
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<td>45</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>5.5 V</td>
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<td>61</td>
<td>51</td>
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<tr>
<td>( t_{en} )</td>
<td>OE</td>
<td>Y</td>
<td>4.5 V</td>
<td>25</td>
<td>52</td>
<td>79</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.5 V</td>
<td>22</td>
<td>47</td>
<td>71</td>
<td>59</td>
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<tr>
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<td>4.5 V</td>
<td>17</td>
<td>42</td>
<td>63</td>
<td>53</td>
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<td>5.5 V</td>
<td>14</td>
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<td>48</td>
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</table>

operating characteristics, \( T_A = 25^\circ\text{C} \)

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<tr>
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<th>TYP</th>
<th>UNIT</th>
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<td>( C_{pd} )</td>
<td>No load</td>
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<td>pF</td>
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**Note:** All parameters are measured with a load capacitance of 150 pF, unless otherwise noted.
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

PARAMETER | R_L | C_L | S1 | S2
---|---|---|---|---
\( t_{en} \) | \( t_{PZH} \) | 1 kΩ | Open | Closed
\( t_{PZL} \) | \( t_{PD} \) | 50 pF or 150 pF | Open | Closed
\( t_{dis} \) | \( t_{PHZ} \) | 1 kΩ | Closed | Open
\( t_{PLZ} \) | \( t_{PL} \) | 50 pF | Closed | Open

NOTES:
A. \( C_L \) includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: \( PRR \leq 1 \text{ MHz} \), \( Z_O = 50 \Omega \), \( t_r = 6 \text{ ns} \), \( t_f = 6 \text{ ns} \).
D. The outputs are measured one at a time with one input transition per measurement.
E. \( t_{PLZ} \) and \( t_{PHZ} \) are the same as \( t_{dis} \).
F. \( t_{PZL} \) and \( t_{PZH} \) are the same as \( t_{en} \).
G. \( t_{PLH} \) and \( t_{PHL} \) are the same as \( t_{pd} \).

Figure 1. Load Circuit and Voltage Waveforms
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
<tr>
<td>5962-8513001VRA</td>
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<td>CDIP</td>
<td>J</td>
<td>20</td>
<td>1</td>
<td>TBD</td>
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<td>N / A for Pkg Type</td>
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<td>5962-8513001VRA SNV54HCT244J Samples</td>
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<tr>
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<td>CFP</td>
<td>W</td>
<td>20</td>
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<td>J</td>
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<td>1</td>
<td>TBD</td>
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<td>TBD</td>
<td>POST-PLATE</td>
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<td>-55 to 125</td>
<td>JM38510/65755B2A Samples</td>
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<tr>
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<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>JM38510/65755BRA Samples</td>
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<td>POST-PLATE</td>
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<td>M38510/65755B2A Samples</td>
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<td>1</td>
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<td>1</td>
<td>TBD</td>
<td>A42</td>
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<td>SN54HCT244J Samples</td>
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<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>HCT244 Samples</td>
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<td>Orderable Device</td>
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<td>Package Type</td>
<td>Package Drawing</td>
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<td>Lead/Ball Finish</td>
<td>MSL Peak Temp</td>
<td>Op Temp (°C)</td>
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<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>8513001RA</td>
<td></td>
</tr>
</tbody>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

---

Addendum-Page 2
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCT244, SN54HCT244-SP, SN74HCT244:
- Catalog: SN74HCT244, SN54HCT244
- Automotive: SN74HCT244-Q1, SN74HCT244-Q1
- Enhanced Product: SN74HCT244-EP, SN74HCT244-EP
Military: SN54HCT244

Space: SN54HCT244-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

![Image of Reel Dimensions]

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Image of Reel Heights]

*All dimensions are nominal.*

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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</table>
J (R-GDIP-T**)

CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Fits within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil-Std 1835 GDFP2–F20
FK (S-CQCC-N**)  
LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

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<td>52</td>
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<td>0.761 (19.32)</td>
<td>0.495 (12.58)</td>
<td>0.560 (14.22)</td>
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<td>0.850 (21.6)</td>
<td>0.858 (21.8)</td>
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<td>1.047 (26.6)</td>
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NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a metal lid.  
D. Falls within JEDEC MS-004
N (R–PDIP–T**)  PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

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<td>BB</td>
<td>AC</td>
<td>AD</td>
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NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).  
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002
NOTES:  
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed $0.006$ (0,15).  
D. Falls within JEDEC MS-013 variation AC.
LAND PATTERN DATA

DW (R-PDSO-G20)  PLASTIC SMALL OUTLINE

Example Board Layout  Stencil Openings
(Note C)  (Note D)

20x0,6  20x0,55
18x1,27  18x1,27
9,4  9,4

Non Solder Mask Define Pad

Solder Mask Opening  Pad Geometry
(Note E)  (Note C)

0,6  2,0
0,07
All Around

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

4209202-4/F  08/13

TEXAS INSTRUMENTS
www.ti.com
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
   △ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
   △ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO–153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
MECHANICAL DATA


DB (R-PDSO-G**)  PLASTIC SMALL-OUTLINE

28 PINS SHOWN

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D.  Falls within JEDEC MO-150

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4040065 /E 12/01
MECHANICAL DATA

NS (R-PDSO-G**)
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

DIMENSIONS:

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<td>12.3</td>
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